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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/964,591	09/28/2001	Akio Matsuda	1075.1174	2406
21171	7590	07/11/2006	EXAMINER	
STAAS & HALSEY LLP SUITE 700 1201 NEW YORK AVENUE, N.W. WASHINGTON, DC 20005			THANGAVELU, KANDASAMY	
			ART UNIT	PAPER NUMBER
			2123	

DATE MAILED: 07/11/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/964,591	MATSUDA ET AL.	
	Examiner Kandasamy Thangavelu	Art Unit 2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) Responsive to communication(s) filed on 17 May 2006.
- 2a) This action is FINAL. 2b) This action is non-final.
- 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) Claim(s) 1-41 is/are pending in the application.
 - 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) Claim(s) _____ is/are allowed.
- 6) Claim(s) 1-41 is/are rejected.
- 7) Claim(s) _____ is/are objected to.
- 8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) The specification is objected to by the Examiner.
- 10) The drawing(s) filed on 28 September 2001 is/are: a) accepted or b) objected to by the Examiner.
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 - a) All b) Some * c) None of:
 1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. _____.
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| <ol style="list-style-type: none"> 1)<input type="checkbox"/> Notice of References Cited (PTO-892) 2)<input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) 3)<input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
 Paper No(s)/Mail Date _____. | <ol style="list-style-type: none"> 4)<input type="checkbox"/> Interview Summary (PTO-413)
 Paper No(s)/Mail Date. _____. 5)<input type="checkbox"/> Notice of Informal Patent Application (PTO-152) 6)<input type="checkbox"/> Other: _____. |
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DETAILED ACTION

1. This communication is in response to the Applicants' Response mailed on May 17, 2006. Claims 1-41 of the application are pending. This office action is made final.

Claim Objections

2. The following is a quotation of 37 C.F.R § 1.75 (d)(1):

The claim or claims must conform to the invention as set forth in the remainder of the specification and terms and phrases in the claims must find clear support or antecedent basis in the description so that the meaning of the terms in the claims may be ascertainable by reference to the description.

3. Claims 1- 41 are objected to because of the following informalities:

3.1 The specification states the following:

Page 7, Lines 17-20: a resource requesting step in which a thread manager, which controls threads each forming an execution unit of a program, **makes a request for a hardware resource** needed for execution of a thread;

Page 7, Lines 23-24: a resource manager which **manages the hardware resource**;

Page 7, Lines 24-25: a resource allocating step in which **the resource manager allocates the hardware resource** meeting the request to the thread;

Page 8, L13-15: the resource manager monitors read/write requests with respect to the **hardware resource allocated by the resource request**;

Page 22, Lines 9-11: each of the processors, ASICs (Application specific integrated circuits), operation units and other units is **defined as resource data**. What is meant by each of the units is defined as resource data? What is the data associated with each of the resources?

Page 22, Line 26 to Page 23, Line 1: The thread manager ... and **allocates a resource 14 corresponding to a resource request**;

Page 23, Lines 23-24: which type of **resource 14 is requested**;

Page 24, Lines 2-3: a function to **arbitrate the resource allocation** at every type of the resource;

Page 24, Lines 14-16: if the number of **resources requested** is 0 or less, then the **resource to be allocated** does not exist;

Page 25, L24-25: the thread 13 which has issued **this resource request**;

Page 26, Lines 4-7: the resource manager ... **allocates the requested resource** to the thread 13;

Page 26, Lines 7-8: while arbitrating **the allocation of resources**;

Page 27, Lines 10-11: on the basis of **the resource request, the resource allocation**;

Page 28, Lines 20-21: **the resource need is dynamically allocated** each time by the resource manager.

The Examiner has checked the full publication of the original patent application with a word processor and determined that there is **no mention of hardware resource data** anywhere in the application. If the applicants disagree, they are directed to show where in the specification the hardware resource data is defined and described.

3.2 Amended Claim 1, Lines 7-10, “a resource manager which manages said hardware resource data:

allocating a resource in which said resource manager allocates said hardware resource data meeting said request to said thread in accordance with a rule prescribed in advance” appears to be incorrect and it appears that it should be “a resource manager which manages said hardware resource;

allocating a resource in which said resource manager allocates said hardware resource meeting said request to said thread in accordance with a rule prescribed in advance”.

Amended Claim 5, Lines 3-7, “with the types of said hardware resources data and are hierarchized according to the dependence among said hardware resources data, and in said resource allocating, the hardware resource data allocation is made in consideration of the dependence between said hardware resource data managed by one of said resource managers and said hardware resource data managed by the other resource manager” appears to be incorrect and it appears that it should be “with the types of said hardware resources and are hierarchized according to the dependence among said hardware resources, and

in said resource allocating, the hardware resource allocation is made in consideration of the dependence between said hardware resource managed by one of said resource managers and said hardware resource managed by the other resource manager”.

Amended Claim 7, Lines 3-5, “said hardware resource data allocated by said resource request in said requesting a resource to make a decision on a competition state in read/write operation on said hardware resource data among a plurality of threads” appears to be incorrect and it appears that it should be “said hardware resource allocated by said resource request in said requesting a resource to make a decision on a competition state in read/write operation on said hardware resource among a plurality of threads”.

Amended Claim 8, Line 3, “with respect to said hardware resource data to detect a bottleneck” appears to be incorrect and it appears that it should be “with respect to said hardware resource to detect a bottleneck”.

Amended Claim 9, Line 3, “with respect to said hardware resource data to detect blocking” appears to be incorrect and it appears that it should be “with respect to said hardware resource to detect blocking”.

Amended Claim 12, Lines 7-10, “a resource manager which manages said hardware resource data;

allocating a resource in which said resource manager allocates said hardware resource data meeting said request to said thread in accordance with a rule prescribed in advance;” appears to be incorrect and it appears that it should be “a resource manager which manages said hardware resource;

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allocating a resource in which said resource manager allocates said hardware resource meeting said request to said thread in accordance with a rule prescribed in advance;”.

Amended Claim 15, Lines 5-6, “each of said resource managers allocates said hardware resource data” appears to be incorrect and it appears that it should be “each of said resource managers allocates said hardware resource”.

Amended Claim 16, Lines 4-8, “according to the dependence among said hardware resources data, and

in said resource allocating, the hardware resource data allocation is made in consideration of the dependence between said hardware resource data managed by one of said resource managers and said hardware resource data managed by the other resource manager” appears to be incorrect and it appears that it should be “according to the dependence among said hardware resources, and

in said resource allocating, the hardware resource allocation is made in consideration of the dependence between said hardware resource managed by one of said resource managers and said hardware resource managed by the other resource manager”.

Amended Claim 18, Lines 3-5, “with respect to said hardware resource data allocated by said resource request in said resource requesting step to make a decision on a competition state in read/write operation on said hardware resource data among a plurality of threads” appears to be incorrect and it appears that it should be “with respect to said hardware resource allocated by

said resource request in said resource requesting step to make a decision on a competition state in read/write operation on said hardware resource among a plurality of threads”.

Amended Claim 19, Line 3, “with respect to said hardware resource data to detect a bottleneck” appears to be incorrect and it appears that it should be “with respect to said hardware resource to detect a bottleneck”.

Amended Claim 20, Line 3, “with respect to said hardware resource data to detect blocking” appears to be incorrect and it appears that it should be “with respect to said hardware resource to detect blocking”.

Amended Claim 24, Lines 5-6, “said hardware resource data” appears to be incorrect and it appears that it should be “said hardware resource”.

Amended Claim 25, Lines 5-8, “said hardware resources data, and in said resource allocating, the hardware resource data allocation is made in consideration of the dependence between said hardware resource data managed by one of said resource managers and said hardware resource data managed by the other resource manager” appears to be incorrect and it appears that it should be “said hardware resources, and

in said resource allocating, the hardware resource allocation is made in consideration of the dependence between said hardware resource managed by one of said resource managers and said hardware resource managed by the other resource manager”.

Amended Claim 27, Lines 3-5, “said hardware resource data allocated by said resource request in said resource requesting to make a decision on a competition state in read/write operation on said hardware resource data among a plurality of threads” appears to be incorrect and it appears that it should be “said hardware resource allocated by said resource request in said resource requesting to make a decision on a competition state in read/write operation on said hardware resource among a plurality of threads”.

Amended Claim 28, Line 3, “said hardware resource data to detect a bottleneck” appears to be incorrect and it appears that it should be “said hardware resource to detect a bottleneck”.

Amended Claim 29, Line 3, “said hardware resource data to detect blocking” appears to be incorrect and it appears that it should be “said hardware resource to detect blocking”.

Amended Claim 33, Lines 5-6, “said hardware resource data” appears to be incorrect and it appears that it should be “said hardware resource”.

Amended Claim 34, Lines 5-8, “among said hardware resources data, and in said resource allocating, the hardware resource data allocation is made in consideration of the dependence between said hardware resource data managed by one of said resource managers and said hardware resource data managed by the other resource manager” appears to be incorrect and it appears that it should be “among said hardware resources, and

in said resource allocating, the hardware resource allocation is made in consideration of the dependence between said hardware resource managed by one of said resource managers and said hardware resource managed by the other resource manager”.

Amended Claim 36, Lines 3-5, “said hardware resource data allocated by said resource request in said resource requesting to make a decision on a competition state in read/write operation on said hardware resource data among a plurality of threads” appears to be incorrect and it appears that it should be “said hardware resource allocated by said resource request in said resource requesting to make a decision on a competition state in read/write operation on said hardware resource among a plurality of threads”.

Amended Claim 37, Line 3, “said hardware resource data” appears to be incorrect and it appears that it should be “said hardware resource”.

Amended Claim 38, Line 3, “said hardware resource data” appears to be incorrect and it appears that it should be “said hardware resource”.

Amended Claim 41, Lines 9-10, “said hardware resource data” appears to be incorrect and it appears that it should be “said hardware resource”.

Claims objected but not specifically addressed are objected based on their dependency on rejected claims.

Appropriate corrections are required.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the first paragraph of 35 U.S.C. §112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

5. Claims 1-41 are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

Amended claim 1 states, “requesting a resource in which a thread manager, which controls threads each forming an execution unit of a program, makes a request for hardware resource data relating to a hardware resource needed for execution of each of threads representative of a series of functions required until the operation of said logical unit reaches completion according to a design specification of said logical unit, to a resource manager which manages said hardware resource data;” and “said thread manager and said resource manager executing said requesting, allocating, and controlling repeatedly in cooperation with each other until the execution of said thread reaches completion while dynamically allocating hardware resource data relating to necessary hardware resources”. There is no support for “making a

request for hardware resource data relating to a hardware resource needed for execution of each of threads” and “dynamically allocating hardware resource data relating to necessary hardware resources” anywhere in the specification. **This is new material added in the amendment and not found in the original specification.** The Examiner directs applicants’ attention to Paragraph 3.1 for further clarification.

Amended claim 10 states, “wherein said thread has a budget on a time of occupancy of hardware resource data relating to a hardware resource allocated by said resource manager”. There is no support for “a budget on a time of occupancy of hardware resource data relating to a hardware resource allocated by said resource manager” anywhere in the specification. This is new material added in the amendment and not found in the original specification.

Amended claim 12 states, “requesting a resource in which a thread manager, which controls threads each forming an execution unit of a program, makes a request for hardware resource data relating to a hardware resource needed for execution of each of threads representative of functions required until the operation of said logical unit reaches completion according to a design specification of said logical unit, to a resource manager which manages said hardware resource data;” and “said thread manager and said resource manager executing said requesting, allocating, and controlling repeatedly in cooperation with each other until the execution of said thread reaches completion while dynamically allocating hardware resource data relating to necessary hardware resources to the thread by said resource manager”. There is no support for “making a request for hardware resource data relating to a hardware resource needed

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for execution of each of threads” and “dynamically allocating hardware resource data relating to necessary hardware resources” anywhere in the specification. This is new material added in the amendment and not found in the original specification.

Amended claim 13 states, “a resource manager for managing hardware resource data relating to a hardware resource needed for execution of said thread”, “resource requesting means for making a request for hardware resource data relating to a hardware resource needed for execution of a thread representative of functions required until the operation of said logical unit reaches completion according to a design specification of said logical unit, to said resource manager”, “resource allocating means for allocating hardware resource data relating to a hardware resource meeting the request to said thread in accordance with a rule prescribed in advance” and “said thread manager and said resource manager conducting the resource request and the control of the thread execution state repeatedly in cooperation with each other until the execution of said thread reaches completion while dynamically allocating hardware resource data relating to necessary hardware resources to the thread by said resource manager”. There is no support for “managing hardware resource data relating to a hardware resource needed for execution of said thread”, “making a request for hardware resource data relating to a hardware resource needed for execution of a thread”, “allocating hardware resource data relating to a hardware resource meeting the request to said thread” and “dynamically allocating hardware resource data relating to necessary hardware resources” anywhere in the specification. This is new material added in the amendment and not found in the original specification.

Amended claim 14 states, “a thread manager for controlling threads each forming an execution unit of said program and as a resource manager for managing hardware resource data relating to a hardware resource needed for execution of each of threads”, “requesting a resource in which said thread manager makes a request for hardware resource data relating to a hardware resource needed for execution of threads” and “said thread manager and said resource manager executing the requesting, the allocating, and the controlling repeatedly in cooperation with each other until the execution of said thread reaches completion while dynamically allocating hardware resource data relating to necessary hardware resources to the thread by said resource manager”. There is no support for “a resource manager for managing hardware resource data relating to a hardware resource needed for execution of each of threads”, “requesting a resource in which said thread manager makes a request for hardware resource data relating to a hardware resource needed for execution of threads” and “dynamically allocating hardware resource data relating to necessary hardware resources” anywhere in the specification. This is new material added in the amendment and not found in the original specification.

Amended claim 15 states, “a plurality of resource managers each corresponding to said resource manager are provided in conjunction with the types of hardware resource data relating to hardware resources”. There is no support for “a plurality of resource managers each corresponding to said resource manager are provided in conjunction with the types of hardware resource data relating to hardware resources” anywhere in the specification. This is new material added in the amendment and not found in the original specification.

Amended claim 16 states, “a plurality of resource managers each corresponding to said resource manager are provided in conjunction with the types of hardware resource data relating to hardware resources and are hierarchized according to the dependence among said hardware resources data”. There is no support for “a plurality of resource managers each corresponding to said resource manager are provided in conjunction with the types of hardware resource data relating to hardware resources and are hierarchized according to the dependence” anywhere in the specification. This is new material added in the amendment and not found in the original specification.

Amended claim 21 states, “said thread has a budget on a time of occupancy of hardware resource data relating to a hardware resource allocated by said resource manager”. There is no support for “a budget on a time of occupancy of hardware resource data relating to a hardware resource allocated by said resource manager” anywhere in the specification. This is new material added in the amendment and not found in the original specification.

Amended claim 24 states, “wherein a plurality of resource managers each corresponding to said resource manager are provided in conjunction with the types of hardware resource data relating to hardware resources”. There is no support for “a plurality of resource managers each corresponding to said resource manager are provided in conjunction with the types of hardware resource data relating to hardware resources” anywhere in the specification. This is new material added in the amendment and not found in the original specification.

Amended claim 25 states, “a plurality of resource managers each corresponding to said resource manager are provided in conjunction with the types of hardware resource data relating to hardware resources and are hierarchized according to the dependence among said hardware resources data”. There is no support for “a plurality of resource managers each corresponding to said resource manager are provided in conjunction with the types of hardware resource data relating to hardware resources” anywhere in the specification. This is new material added in the amendment and not found in the original specification.

Amended claim 30 states, “said thread has a budget on a time of occupancy of hardware resource data relating to a hardware resource allocated by said resource manager”. There is no support for “thread has a budget on a time of occupancy of hardware resource data relating to a hardware resource allocated by said resource manager” anywhere in the specification. This is new material added in the amendment and not found in the original specification.

Amended claim 33 states, “a plurality of resource managers each corresponding to said resource manager are provided in conjunction with the types of hardware resource data relating to hardware resources”. There is no support for “a plurality of resource managers each corresponding to said resource manager are provided in conjunction with the types of hardware resource data relating to hardware resources” anywhere in the specification. This is new material added in the amendment and not found in the original specification.

Amended claim 34 states, “a plurality of resource managers each corresponding to said resource manager are provided in conjunction with the types of hardware resource data relating to hardware resources and are hierarchized according to the dependence among said hardware resources data”. There is no support for “a plurality of resource managers each corresponding to said resource manager are provided in conjunction with the types of hardware resource data relating to hardware resources and are hierarchized according to the dependence among said hardware resources data” anywhere in the specification. This is new material added in the amendment and not found in the original specification.

Amended claim 39 states, “said thread has a budget on a time of occupancy of hardware resource data relating to a hardware resource allocated by said resource manager”. There is no support for “said thread has a budget on a time of occupancy of hardware resource data relating to a hardware resource allocated by said resource manager” anywhere in the specification. This is new material added in the amendment and not found in the original specification.

Amended claim 41 states, “requesting a resource in which a thread manager, which controls threads each forming an execution unit of a program, makes a request for hardware resource data relating to a hardware resource needed for execution of each of threads representative of functions required until the operation of said logical unit reaches completion according to a design specification of said logical unit, to a resource manager which manages said hardware resource data;” and “said thread manager and said resource manager executing the requesting, the allocating, and the controlling repeatedly in cooperation with each other until the

execution of said thread reaches completion while dynamically allocating hardware resource data relating to necessary hardware resources to the thread by said resource manager every time the generated thread is executed, simulating the operation of said logical unit to be conducted up to the completion”. There is no support for “making a request for hardware resource data relating to a hardware resource needed for execution of each of threads “, and “dynamically allocating hardware resource data relating to necessary hardware resources to the thread by said resource manager” anywhere in the specification. This is new material added in the amendment and not found in the original specification.

Claims rejected but not specifically addressed are rejected based on their dependency on rejected claims.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains.

7. The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

8. Claims 1, 3, 6, 13, 14, 17, 32 and 35 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Chen** (U.S. Patent 6,466,898) in view of **Dearth et al.** (U.S. Patent 6,345,242), and further in view of **Dearth et al.** (U.S. Patent 5,812,824) and **Levy et al.** (U.S. Patent 6,092,175).

8.1 **Chen** teaches multithreaded, mixed hardware description language logic simulation on engineering workstations. Specifically as per claim 1, **Chen** teaches a method of simulating an operation of a logical unit (CL1, L1-3; CL1, L12-15; CL3, L10-11; CL3, L18-20).

Chen teaches a thread manager, which controls threads each forming an execution unit of a program, for execution of each of threads representative of a series of functions required until the operation of the logical unit reaches completion according to a design specification of the logical unit (Fig 8 and Fig. 11). **Chen** does not expressly teach requesting a resource in which a thread manager makes a request for hardware resource data relating to a hardware resource needed for execution of each of threads, to a resource manager which manages the hardware resource data. **Dearth et al.** ('242) teaches requesting a resource in which a thread manager makes a request for hardware resource data relating to a hardware resource needed for execution of each of threads, to a resource manager which manages the hardware resource data (Fig. 2,

Item 202 and Item 130; Abstract L17-20). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the method of **Chen** with the method of **Dearth et al.** ('242) that included requesting a resource in which a thread manager makes a request for hardware resource data relating to a hardware resource needed for execution of each of threads, to a resource manager which manages the hardware resource data because as per **Dearth et al.** ('824), when simulating a circuit using multiple concurrently executing threads, often more than one thread would attempt to interact with the same simulated component of the simulated circuit or device; and it would be necessary to avoid collisions in multiple concurrently executing threads by reserving simulated devices to one or more simulation threads (CL2, L30-33; Abstract, L1-3; CL4, L32-36).

Chen does not expressly teach allocating a resource in which the resource manager allocates the hardware resource data meeting the request to the thread in accordance with a rule prescribed in advance. **Dearth et al.** ('824) teaches allocating a resource in which the resource manager allocates the hardware resource data meeting the request to the thread in accordance with a rule prescribed in advance (CL2, L46-48). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the method of **Chen** with the method of **Dearth et al.** ('242) that included allocating a resource in which the resource manager allocates the hardware resource data meeting the request to the thread in accordance with a rule prescribed in advance because when simulating a circuit using multiple concurrently executing threads, often more than one thread would attempt to interact with the same simulated component of the simulated circuit or device; and it would be necessary to avoid collisions in

multiple concurrently executing threads by reserving simulated devices to one or more simulation threads (CL2, L30-33; Abstract, L1-3; CL4, L32-36).

Chen teaches controlling a thread in which the thread manager controls an execution state of the thread, the thread manager executing the requesting, allocating, and controlling repeatedly until the execution of the thread reaches completion, for simulating the operation of the logical unit to be conducted up to the completion (Fig 8 and Fig. 11). **Chen** does not expressly teach controlling a thread in which the thread manager controls an execution state of the thread in accordance with a result of the allocation made by the resource manager, the thread manager and the resource manager executing the requesting, allocating, and controlling repeatedly in cooperation with each other until the execution of the thread reaches completion simulating the operation of the logical unit to be conducted up to the completion. **Dearth et al.** ('242) teaches controlling a thread in which the thread manager controls an execution state of the thread in accordance with a result of the allocation made by the resource manager, the thread manager and the resource manager executing the requesting, allocating, and controlling repeatedly in cooperation with each other until the execution of the thread reaches completion simulating the operation of the logical unit to be conducted up to the completion (Fig. 2; Abstract L22-26).

Chen does not expressly teach dynamically allocating hardware resource data relating to necessary hardware resources to the thread by the resource manager every time the generated thread is executed. **Levy et al.** teaches dynamically allocating hardware resource data relating to necessary hardware resources to the thread by the resource manager every time the generated thread is executed (CL3, L11-15; CL3, L22-30; CL3, L35-45). It would have been obvious to

one of ordinary skill in the art at the time of Applicants' invention to modify the method of **Chen** with the method of **Levy et al.** that included dynamically allocating hardware resource data relating to necessary hardware resources to the thread by the resource manager every time the generated thread is executed because that would support out-of-order execution of instructions for the threads (CL3, L14-15) with dynamic scheduling of instructions thus improving the performance of multithreaded processor (CL1, L38-41).

8.2 As per claim 3, **Chen**, **Dearth et al.** ('242), **Dearth et al.** ('824) and **Levy et al.** teach the method of claim 1. **Chen** teaches that the series of functions are represented in a plurality of sequential or concurrently executed threads (Fig. 8 and Fig 11).

8.3 As per claim 6, **Chen**, **Dearth et al.** ('242), **Dearth et al.** ('824) and **Levy et al.** teach the method of claim 1. **Chen** does not expressly teach that the resource manager monitors resource requests in the requesting a resource to make a decision on a resource request deadlock state among a plurality of threads as a result of the monitoring. **Dearth et al.** ('824) teaches that the resource manager monitors resource requests in the requesting a resource to make a decision on a resource request deadlock state among a plurality of threads as a result of the monitoring (Abstract, L3-7; CL2, L30-33; CL3, L1-6).

8.4 As per claim 13, **Chen** teaches an apparatus for simulating an operation of a logical unit (CL1, L1-3; CL1, L12-15; CL3, L10-11; CL3, L18-20); comprising:

Chen teaches a thread manager for controlling a thread forming an execution unit of a program (Fig 8 and Fig. 11).

Chen does not expressly teach a resource manager for managing hardware resource data relating to a hardware resource needed for execution of the thread; and resource allocating means for allocating hardware resource data relating to a hardware resource meeting the request to the thread in accordance with a rule prescribed in advance. **Dearth et al.** ('824) teaches a resource manager for managing hardware resource data relating to a hardware resource needed for execution of the thread; and resource allocating means for allocating hardware resource data relating to a hardware resource meeting the request to the thread in accordance with a rule prescribed in advance (CL2, L46-48).

Chen teaches a thread manager for execution of a thread representative of functions required until the operation of the logical unit reaches completion according to a design specification of the logical unit (Fig 8 and Fig. 11). **Chen** does not expressly teach resource requesting means for making a request for hardware resource data relating to a hardware resource needed for execution of a thread to the resource manager. **Dearth et al.** ('242) teaches resource requesting means for making a request for hardware resource data relating to a hardware resource needed for execution of a thread to the resource manager (Fig. 2, Item 202 and Item 130; Abstract L17-20).

Chen teaches thread control means for controlling an execution state of the thread; and the thread manager conducting the control of the thread execution state repeatedly in cooperation with each other until the execution of the thread reaches completion, for simulating the operation

of the logical unit to be conducted up to the completion (Fig 8 and Fig. 11). **Chen** does not expressly teach thread control means for controlling an execution state of the thread in accordance with a result of a resource allocation made by the resource manager in response to the request from the resource requesting means; and the thread manager and the resource manager conducting the resource request and the control of the thread execution state repeatedly in cooperation with each other. **Dearth et al.** ('242) teaches thread control means for controlling an execution state of the thread in accordance with a result of a resource allocation made by the resource manager in response to the request from the resource requesting means; and the thread manager and the resource manager conducting the resource request and the control of the thread execution state repeatedly in cooperation with each other (Fig. 2; Abstract L22-26).

Chen does not expressly teach dynamically allocating hardware resource data relating to necessary hardware resources to the thread by the resource manager every time the generated thread is executed. **Levy et al.** teaches dynamically allocating hardware resource data relating to necessary hardware resources to the thread by the resource manager every time the generated thread is executed (CL3, L11-15; CL3, L22-30; CL3, L35-45).

8.5 As per Claim 14, it is rejected based on the same reasoning as Claim 13, supra. Claim 14 is a computer readable recording medium claim reciting the same limitations as Claim 13, as taught throughout by **Chen**, **Dearth et al.** ('242), **Dearth et al.** ('824) and **Levy et al.**

8.6 As per Claims 17 and 35, these are rejected based on the same reasoning as Claim 6, supra. Claims 17 and 35 are computer readable recording medium claims reciting the same

limitations as Claim 6, as taught throughout by **Chen, Dearth et al.** ('242), **Dearth et al.** ('824) and **Levy et al.**

8.7 As per Claim 32, it is rejected based on the same reasoning as Claim 3, supra. Claim 32 is a computer readable recording medium claim reciting the same limitations as Claim 3, as taught throughout by **Chen, Dearth et al.** ('242), **Dearth et al.** ('824) and **Levy et al.**

9. Claims 2, 23 and 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Chen** (U.S. Patent 6,466,898) in view of **Dearth et al.** (U.S. Patent 6,345,242), **Dearth et al.** (U.S. Patent 5,812,824) and **Levy et al.** (U.S. Patent 6,092,175), and further in view of **Kinzelman et al.** (U.S. Patent 5,594,741).

9.1 As per claim 2, **Chen, Dearth et al.** ('242), **Dearth et al.** ('824) and **Levy et al.** teach the method of claim 1. **Chen** does not expressly teach that the series of functions are represented in a plurality of sequential threads. **Kinzelman et al.** teaches that the series of functions are represented in a plurality of sequential threads (CL8, L49-52; CL11, L13-17). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the method of **Chen** with the method of **Kinzelman et al.** that included the series of functions being represented in a plurality of sequential threads because that would allow instruction threads to be synchronized to align responder instructions from one transactor with the appropriate commander instructions (CL8, L46-49).

9.2 As per claim 23, **Chen, Dearth et al.** ('242), **Dearth et al.** ('824) and **Levy et al.** teach the computer readable medium of claim 14. **Chen** does not expressly teach that the series of functions are represented in a plurality of sequential threads. **Kinzelman et al.** teaches that the series of functions are represented in a plurality of sequential threads (CL8, L49-52; CL11, L13-17).

9.3 As per claim 26, **Chen, Dearth et al.** ('242), **Dearth et al.** ('824), **Levy et al.** and **Kinzelman et al.** teach the computer readable medium of claim 23. **Claim 26** has same limitations as Claim 17.

10. Claims 4, 5, 15, 16, 33 and 34 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Chen** (U.S. Patent 6,466,898) in view of **Dearth et al.** (U.S. Patent 6,345,242), **Dearth et al.** (U.S. Patent 5,812,824) and **Levy et al.** (U.S. Patent 6,092,175), and further in view of **De Yong et al.** (U.S. Patent 5,355,435).

10.1 As per claim 4, **Chen, Dearth et al.** ('242), **Dearth et al.** ('824) and **Levy et al.** teach the method of claim 1. **Chen** does not expressly teach that a plurality of resource managers each corresponding to the resource manager are provided in conjunction with the types of the hardware resources data, and in the allocating a resource, each of the resource managers allocates the hardware resource data, the resource manager manages, to the thread in accordance with a local rule described in advance. **Dearth et al.** ('824) teaches that a resource manager is provided in conjunction with the types of the hardware resources data, and in the allocating a resource, the

resource manager allocates the hardware resource data, the resource manager manages, to the thread in accordance with a local rule described in advance (Abstract, L1-9; CL1, L40-44; CL2, L46-48).

Chen does not expressly teach a plurality of resource managers each corresponding to the resource manager are provided in conjunction with the types of the hardware resources. **De Yong et al.** teaches a plurality of resource managers each corresponding to the resource manager are provided in conjunction with the types of the hardware resources (CL19, L35-36), because a plurality of hierarchical resource managers (arbitration systems) provide an ordered resolution of temporal contentions (CL19, L35-36). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the method of **Chen** with the method of **De Yong et al.** that included a plurality of resource managers each corresponding to the resource manager are provided in conjunction with the types of the hardware resources. The artisan would have been motivated because a plurality of hierarchical resource managers (arbitration systems) would provide an ordered resolution of temporal contentions.

10.2 As per claim 5, **Chen**, **Dearth et al.** ('242), **Dearth et al.** ('824) and **Levy et al.** teach the method of claim 1. **Chen** does not expressly teach a plurality of resource managers each corresponding to the resource manager are provided in conjunction with the types of the hardware resources data and are hierarchized according to the dependence among the hardware resources data, and in the resource allocating, the hardware resource data allocation is made in consideration of the dependence between the hardware resource data managed by one of the resource managers and the hardware resource managed by the other resource manager lower in

hierarchy than the one of the resource managers. **De Yong et al.** teaches a plurality of resource managers each corresponding to the resource manager are provided in conjunction with the types of the hardware resources data and are hierarchized according to the dependence among the hardware resources data, and in the resource allocating, the hardware resource data allocation is made in consideration of the dependence between the hardware resource data managed by one of the resource managers and the hardware resource managed by the other resource manager lower in hierarchy than the one of the resource managers (CL19, L35-36). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the method of **Chen** with the method of **De Yong et al.** that included a plurality of resource managers each corresponding to the resource manager would be provided in conjunction with the types of the hardware resources data and would be hierarchized according to the dependence among the hardware resources data, and in the resource allocating, the hardware resource data allocation would be made in consideration of the dependence between the hardware resource data managed by one of the resource managers and the hardware resource managed by the other resource manager lower in hierarchy than the one of the resource managers because a plurality of hierarchical resource managers (arbitration systems) would provide an ordered resolution of temporal contentions (CL19, L35-36).

10.3 As per Claims 15, 16, 33 and 34, these are rejected based on the same reasoning as Claims 4 and 5, supra. Claims 15, 16, 33 and 34 are a computer readable recording medium claim reciting the same limitations as Claims 4 and 5, as taught throughout by **Chen, Dearth et al.** ('242), **Dearth et al.** ('824), **Levy et al.** and **De Yong et al.**

11. Claims 7, 18 and 36 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Chen** (U.S. Patent 6,466,898) in view of **Dearth et al.** (U.S. Patent 6,345,242), **Dearth et al.** (U.S. Patent 5,812,824) and **Levy et al.** (U.S. Patent 6,092,175), and further in view of **Thekkath et al.** (U.S. Patent 6,490,642).

11.1 As per claim 7, **Chen**, **Dearth et al.** ('242), **Dearth et al.** ('824) and **Levy et al.** teach the method of claim 1. **Chen** does not expressly teach that the resource manager monitors read/write requests with respect to the hardware resource data allocated by the resource request in the requesting a resource to make a decision on a competition state in read/write operation on the hardware resource data among a plurality of threads on the basis of a result of the monitoring. **Dearth et al.** ('824) teaches that the resource manager monitors requests with respect to the hardware resource data allocated by the resource request in the requesting a resource to make a decision on a competition state in operation on the hardware resource data among a plurality of threads on the basis of a result of the monitoring (Abstract, L1-3; CL2, L30-33).

Chen does not expressly teach that the resource manager monitors read/write requests with respect to the hardware resource data allocated by the resource request in the resource requesting step to make a decision on a competition state in read/write operation on the hardware resource data among a plurality of threads on the basis of a result of the monitoring. **Thekkath et al.** teaches that the resource manager monitors read/write requests with respect to the hardware resource data allocated by the resource request in the resource requesting step to make a decision on a competition state in read/write operation on the hardware resource data among a

plurality of threads on the basis of a result of the monitoring (Abstract, L8-18; CL2, L23-34; CL2, L48-64; CL6, L65 to CL7, L5; CL9, L53-59). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the method of **Chen** with the method of **Thekkath et al.** that included the resource manager monitoring read/write requests with respect to the hardware resource data allocated by the resource request in the resource requesting step to make a decision on a competition state in read/write operation on the hardware resource data among a plurality of threads on the basis of a result of the monitoring because that would allow improving the efficiency of data transfers between devices interconnected over a system bus in a multi-master computer system configuration (Abstract, L1-4).

11.2 As per Claims 18 and 36, it is rejected based on the same reasoning as Claim 7, supra. Claims 18 and 36 are computer readable recording medium claims reciting the same limitations as Claim 7, as taught throughout by **Chen**, **Dearth et al.** ('242), **Dearth et al.** ('824), **Levy et al.** and **Thekkath et al.**.

12. Claims 8, 10, 19, 21, 37 and 39 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Chen** (U.S. Patent 6,466,898) in view of **Dearth et al.** (U.S. Patent 6,345,242), **Dearth et al.** (U.S. Patent 5,812,824) and **Levy et al.** (U.S. Patent 6,092,175), and further in view of **Markov** (U.S. Patent 6,314,552).

12.1 As per claim 8, **Chen, Dearth et al.** ('242), **Dearth et al.** ('824) and **Levy et al.** teach the method of claim 1. **Chen** does not expressly teach that the resource manager monitors the number of resource requests with respect to the hardware resource data to detect a bottleneck on the thread on the basis of a result of the monitoring. **Markov** teaches that the resource manager monitors the number of resource requests with respect to the hardware resource data to detect a bottleneck on the thread on the basis of a result of the monitoring (CL7, L27-34). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the method of **Chen** with the method of **Markov** that included the resource manager monitoring the number of resource requests with respect to the hardware resource data to detect a bottleneck on the thread on the basis of a result of the monitoring because that would allow the resource manager to intervene and control the bottlenecks and allow evolutionary generation of candidate architectures (CL6, L7-12).

12.2 As per claim 10, **Chen, Dearth et al.** ('242), **Dearth et al.** ('824) and **Levy et al.** teach the method of claim 1. **Chen** does not expressly teach that the thread has a budget on a time of occupancy of hardware resource data relating to a hardware resource allocated by the resource manager. **Markov** teaches that the thread has a budget on a time of occupancy of hardware resource data relating to a hardware resource allocated by the resource manager (CL7, L27-34).

12.3 As per Claims 19, 21, 37 and 39, these are rejected based on the same reasoning as Claims 8 and 10, supra. Claims 19, 21, 37 and 39 are computer readable recording medium

claims reciting the same limitations as Claims 8 and 10, as taught throughout by **Chen, Dearth et al.** ('242), **Dearth et al.** ('824), **Levy et al.** and **Markov**.

13. Claims 9, 20 and 38 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Chen** (U.S. Patent 6,466,898) in view of **Dearth et al.** (U.S. Patent 6,345,242), **Dearth et al.** (U.S. Patent 5,812,824) and **Levy et al.** (U.S. Patent 6,092,175), and further in view of **Markov** (U.S. Patent 6,314,552) and **Kasuya** (U.S. Patent 6,077,304).

13.1 As per claim 9, **Chen, Dearth et al.** ('242), **Dearth et al.** ('824) and **Levy et al.** teach the method of claim 1. **Chen** does not expressly teach that the resource manager monitors the number of resource requests with respect to the hardware resource data to detect blocking of the resource requests on the basis of a result of the monitoring. **Kasuya** teaches that the resource manager monitors the number of resource requests with respect to the hardware resource data to detect blocking of the resource requests on the basis of a result of the monitoring (Abstract, L12-16). (CL6, L7-12). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the method of **Chen** with the method of **Kasuya** that included the resource manager monitoring the number of resource requests with respect to the hardware resource data to detect blocking of the resource requests on the basis of a result of the monitoring because as per **Markov** that would allow the resource manager to intervene and control the blocking and allow evolutionary generation of candidate architectures.

13.2 As per Claims 20 and 38, these are rejected based on the same reasoning as Claim 9, supra. Claims 20 and 38 are computer readable recording medium claims reciting the same limitations as Claim 9, as taught throughout by **Chen, Dearth et al.** ('242), **Dearth et al.** ('824), **Levy et al.**, **Markov** and **Kasuya**.

14. Claims 11, 22 and 40 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Chen** (U.S. Patent 6,466,898) in view of **Dearth et al.** (U.S. Patent 6,345,242), **Dearth et al.** (U.S. Patent 5,812,824) and **Levy et al.** (U.S. Patent 6,092,175), and further in view of **Furuichi** (U.S. Patent 5,437,037).

14.1 As per claim 11, **Chen, Dearth et al.** ('242), **Dearth et al.** ('824) and **Levy et al.** teach the method of claim 1. **Chen** does not expressly teach that the thread has an execution time-limit on the function. **Furuichi** teaches that the thread has an execution time-limit on the function (CL2, L34-36). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the method of **Chen** with the method of **Furuichi** that included the thread having an execution time-limit on the function because as per **Dearth et al.** ('824) that would allow collision in access to a simulated processor to be avoided by reserving the simulated device to the concurrently executing threads for specific time period (Abstract, L1-3; CL2, L30-33).

14.2 As per Claims 22 and 40, these are rejected based on the same reasoning as Claim 11, supra. Claims 22 and 40 are computer readable recording medium claims reciting the same

limitations as Claim 11, as taught throughout by **Chen, Dearth et al.** ('242), **Dearth et al.** ('824), **Levy et al.** and **Furuichi**.

15. Claims 12 and 41 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Chen** (U.S. Patent 6,466,898) in view of **Dearth et al.** (U.S. Patent 6,345,242), **Dearth et al.** (U.S. Patent 5,812,824) and **Levy et al.** (U.S. Patent 6,092,175), and further in view of **Hollander** (U.S. Patent 6,347,388).

15.1 As per claim 12, **Chen** teaches a method of simulating an operation of a logical unit (CL1, L1-3; CL1, L12-15; CL3, L10-11; CL3, L18-20).

Chen teaches a thread manager, which controls threads each forming an execution unit of a program, for execution of each of a series of threads representative of functions required until the operation of the logical unit reaches completion according to a design specification of the logical unit (Fig 8 and Fig. 11). **Chen** does not expressly teach requesting a resource in which a thread manager makes a request for hardware resource data relating to a hardware resource needed for execution of each of a series of threads, to a resource manager which manages the hardware resource data. **Dearth et al.** ('242) teaches requesting a resource in which a thread manager makes a request for hardware resource data relating to a hardware resource needed for execution of each of a series of threads, to a resource manager which manages the hardware resource data (Fig. 2, Item 202 and Item 130; Abstract L17-20).

Chen does not expressly teach allocating a resource in which the resource manager allocates the hardware resource data meeting the request to the thread in accordance with a rule prescribed in advance. **Dearth et al.** ('824) teaches allocating a resource in which the resource manager allocates the hardware resource data meeting the request to the thread in accordance with a rule prescribed in advance (CL2, L46-48).

Chen teaches controlling a thread in which the thread manager controls an execution state of the thread, the thread manager executing the requesting, allocating, and controlling repeatedly until the execution of the thread reaches completion, for simulating the operation of the logical unit to be conducted up to the completion (Fig 8 and Fig. 11). **Chen** does not expressly teach controlling a thread in which the thread manager controls an execution state of the thread in accordance with a result of the allocation made by the resource manager, the thread manager and the resource manager executing the requesting, allocating, and controlling repeatedly in cooperation with each other until the execution of the thread reaches completion simulating the operation of the logical unit to be conducted up to the completion. **Dearth et al.** ('242) teaches controlling a thread in which the thread manager controls an execution state of the thread in accordance with a result of the allocation made by the resource manager, the thread manager and the resource manager executing the requesting, allocating, and controlling repeatedly in cooperation with each other until the execution of the thread reaches completion simulating the operation of the logical unit to be conducted up to the completion (Fig. 2; Abstract L22-26).

Chen does not expressly teach dynamically allocating hardware resource data relating to necessary hardware resources to the thread by the resource manager every time the generated

thread is executed. **Levy et al.** teaches dynamically allocating hardware resource data relating to necessary hardware resources to the thread by the resource manager every time the generated thread is executed (CL3, L11-15; CL3, L22-30; CL3, L35-45).

Chen does not expressly teach comparing a result of the simulation with an estimated value on the operation of the logical unit. **Hollander** teaches comparing a result of the simulation with an estimated value on the operation of the logical unit (CL1, L53-55; CL1, L66-67). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the method of **Chen** with the method of **Hollander** that included comparing a result of the simulation with an estimated value on the operation of the logical unit because that would allow the designer to determine whether a particular hardware and software combination exactly implements the requirements defined by the IC's specification (CL1, L15-18).

Chen does not expressly teach outputting a result of the comparison to an external unit. **Hollander** teaches outputting a result of the comparison to an external unit (CL2, L25-27; CL2, L33-34).

15.2 As per Claim 41, it is rejected based on the same reasoning as Claim 12, supra. Claim 41 is a computer readable recording medium claim reciting the same limitations as Claim 11, as taught throughout by **Chen, Dearth et al.** ('242), **Dearth et al.** ('824), **Levy et al.** and **Hollander**.

16. Claims 24 and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Chen** (U.S. Patent 6,466,898) in view of **Dearth et al.** (U.S. Patent 6,345,242), **Dearth et al.** (U.S.

Patent 5,812,824) and **Levy et al.** (U.S. Patent 6,092,175), and further in view of **Kinzelman et al.** (U.S. Patent 5,594,741) and **De Yong et al.** (U.S. Patent 5,355,435)

16.1 As per claim 24, **Chen, Dearth et al.** ('242), **Dearth et al.** ('824), **Levy et al.** and **Kinzelman et al.** teach the computer readable medium of claim 23. Claim 24 has same limitation as claim 15, which is taught by **De Yong et al.**

16.2 As per claim 25, **Chen, Dearth et al.** ('242), **Dearth et al.** ('824), **Levy et al.** and **Kinzelman et al.** teach the computer readable medium of claim 23. Claim 25 has same limitation as claim 16, which is taught by **De Yong et al.**

17. Claim 27 is rejected under 35 U.S.C. 103(a) as being unpatentable over **Chen** (U.S. Patent 6,466,898) in view of **Dearth et al.** (U.S. Patent 6,345,242), **Dearth et al.** (U.S. Patent 5,812,824) and **Levy et al.** (U.S. Patent 6,092,175), and further in view of **Kinzelman et al.** (U.S. Patent 5,594,741) and **Thekkath et al.** (U.S. Patent 6,490,642).

17.1 As per claim 27, **Chen, Dearth et al.** ('242), **Dearth et al.** ('824), **Levy et al.** and **Kinzelman et al.** teach the computer readable medium of claim 23. Claim 27 has same limitation as claim 18, which is taught by **Thekkath et al.**

18. Claims 28 and 30 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Chen** (U.S. Patent 6,466,898) in view of **Dearth et al.** (U.S. Patent 6,345,242), and **Dearth et al.** (U.S.

Patent 5,812,824), and further in view of **Kinzelman et al.** (U.S. Patent 5,594,741) and **Markov** (U.S. Patent 6,314,552).

18.1 As per claims 28 and 30, **Chen, Dearth et al.** ('242), **Dearth et al.** ('824), **Levy et al.** and **Kinzelman et al.** teach the computer readable medium of claim 23. claims 28 and 30 have same limitations as claim 8 and 10, which are taught by **Markov**.

19. Claim 29 is rejected under 35 U.S.C. 103(a) as being unpatentable over **Chen** (U.S. Patent 6,466,898) in view of **Dearth et al.** (U.S. Patent 6,345,242), **Dearth et al.** (U.S. Patent 5,812,824) and **Levy et al.** (U.S. Patent 6,092,175), and further in view of **Kinzelman et al.** (U.S. Patent 5,594,741), **Markov** (U.S. Patent 6,314,552) and **Kasuya** (U.S. Patent 6,077,304).

19.1 As per claim 29, **Chen, Dearth et al.** ('242), **Dearth et al.** ('824), **Levy et al.** and **Kinzelman et al.** teach the computer readable medium of claim 23. Claim 29 has same limitation as claim 20, which is taught by **Markov** and **Kasuya**.

20. Claim 31 is are rejected under 35 U.S.C. 103(a) as being unpatentable over **Chen** (U.S. Patent 6,466,898) in view of **Dearth et al.** (U.S. Patent 6,345,242), **Dearth et al.** (U.S. Patent 5,812,824) and **Levy et al.** (U.S. Patent 6,092,175), and further in view of **Kinzelman et al.** (U.S. Patent 5,594,741) and **Furuichi** (U.S. Patent 5,437,037).

20.1 As per claim 31, **Chen, Dearth et al.** ('242), **Dearth et al.** ('824), **Levy et al.** and **Kinzelman et al.** teach the computer readable medium of claim 23. Claim 31 has same limitation as claim 22, which is taught by **Furuichi**.

Response to Arguments

21. Applicants' arguments filed on May 17, 2006 have been fully considered. The arguments with respect to 103 (a) rejections are not persuasive.

21.1 As per the applicants' argument that "the Examiner objects to claims 1- 41 because of informalities; the Examiner contends "a resource manager which manages said hardware resource lea allocating a resource in which said resource manager allocates said hardware resource data meeting said request to said thread in accordance with a rule prescribed In advance" appears to be Incorrect and it appears that it should be "a resource manager which manages said hardware resource";

the Examiner rejects claims 141 under 35 U.S.C. §112, first paragraph contending the claims 1-41 contain subject matter that was not described in the specification; the Examiner contends that there is no support for "making a request for hardware resource data relating to, a hardware resource needed for execution of each of threads" and "dynamically allocating hardware resource data relating to necessary hardware resources" anywhere in the specification; this is new material added in the amendment (filed May 10, 2005) and not found in the original specification;

Applicants submit that the Examiner's contentions are not correct and that claims 1-41 are correct and **properly supported as currently written**; Applicants respectfully point out, for example, that as discussed in paragraph [0051] the resource 14 signifies information about a hardware resource; for example, each of processors, ASICs (Application Specific Integrated Circuits), **operation units and other units is defined as resource data**;

and in paragraph [0054] that (t)he resource manager 12 **manages resources** 14 (type and number) needed for the progress of the threads 13 (the execution of the 'methods"), and **allocates a resource** 14 cor'espnding to a resource request 19 to the request issuing thread 13;

That is, the specification specifically discusses and **provides the required support for claims 1-41**, i.e., a resource manager that manages information about a hardware resource that is hardware resource data (resource 14); Applicants submit that **claims 1-41 comply 35 U.S.C. §112, first paragraph** and request the objection and rejection by withdrawn;

the Examiner **incorrectly contends** applicants have introduced the term "hardware resource data" in this (previous) amendment; however, such a term was not used in the original application and hence is new material introduced, which is not allowed at this stage of prosecution", the examiner respectfully disagrees.

As stated in Paragraph 3.1 above, the original specification does not have any reference to hardware reference data, as verified by a full word search of the complete application. The applicants have introduced the term "hardware resource data" in the amendment of May 2005. Since this is new material introduced, it is not allowed at this stage of prosecution. If the applicants disagree with the Examiner, they are directed to show where in the specification

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allocation of hardware reference data is described. Additionally, the specification does not describe anywhere what is meant by hardware resource data and what data is associated with hardware resource.

Therefore, the Examiner does not agree to withdraw the objections and rejections under 35 USC 112 first Paragraph of claims 1-41.

21.2 As per the applicants' argument that "the Examiner also incorrectly concludes that since Levy teaches a resource is dynamically allocated that there is no difference between what the applicants are claiming and what the Dearth et al. (242), and Dearth et al. (824) references teach for the simulation; the Examiner bases this **incorrect conclusion** on the contention that in any simulation, the real hardware will be assigned for executing the threads; the resource manager does not assign data but the resources and that Dearth et al. ('242), and Dearth et al. ('824) references use distributed simulation and assign the resources to multiple threads in distributed simulation; the resources allocated are real resources and not data; Applicants submit that features recited by each of the independent claims, using claim 1 as an example, that a method of simulating an operation of a logical unit allocating hardware resource data relating to necessary hardware resources are not taught by the cited art, alone or in combination", the examiner respectfully disagrees.

Applicants' attention is directed to paragraph 21.1 above.

Dearth et al. ('242) teaches requesting a resource in which a thread manager makes a request for hardware resource relating to a hardware resource needed for execution of each of threads, to a resource manager which manages the hardware resource (Fig. 2, Item 202 and Item

130; Abstract L17-20). **Dearth et al.** ('824) teaches allocating a resource in which the resource manager allocates the hardware resource meeting the request to the thread in accordance with a rule prescribed in advance (CL2, L46-48). **Dearth et al.** ('242) teaches controlling a thread in which the thread manager controls an execution state of the thread in accordance with a result of the allocation made by the resource manager, the thread manager and the resource manager executing the requesting, allocating, and controlling repeatedly in cooperation with each other until the execution of the thread reaches completion simulating the operation of the logical unit to be conducted up to the completion (Fig. 2; Abstract L22-26). **Levy et al.** teaches dynamically allocating hardware resource relating to necessary hardware resources to the thread by the resource manager every time the generated thread is executed (CL3, L11-15; CL3, L22-30; CL3, L35-45).

21.3 As per the applicants' argument that "Applicants submit that the Examiner's conclusion given his arguments is incorrect; the Examiner appears to be contending that in essence that 1) since the cited references teach a resource manager manages hardware resources and does not assign data, that it is understood that by those skilled in the art that a resource manager manages hardware resources and thus 2) claims 1-41 should be rejected; none of the cited art, alone or in combination teach a simulation using hardware resource data relating to necessary hardware resources as recited in each of the independent claims", the examiner respectfully disagrees. Applicants' attention is directed to paragraphs 21.1 and 21.2 above.

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21.4 As per the applicants' argument that "Levy does not teach a technique of a simulation of a logical unit but rather renaming of actual registers; the simulations taught by Dearth '242 and Dearth '824 do not teach allocation of data", the examiner respectfully disagrees. Applicants' attention is directed to paragraphs 21.2 above.

21.5 As per the applicants' argument that "the Examiner's statement that "in any simulation, the real hardware will be assigned for executing the threads" is without support, and that appropriate support should be provided or the rejections withdrawn; The Applicants demand the Examiner produce authority for the statement; the noticed fact is not considered to be common knowledge or well-known in the art; in this case, the limitation is not of notorious character or capable of instant and unquestionable demonstration as being well-known; instead, this limitation is unique to the present invention; further, there is no evidence supporting the Examiner's assertion; in addition, it appears that the Examiner also bases the rejection, at least in part, on personal knowledge; the Examiner is required under 37 C.F.R. § I .104(d)(2) to support such an assertion with an affidavit when called for by the Applicant; thus, Applicants call upon the Examiner to support such assertion with an affidavit", the examiner provides the following art references to assert his position that "in any simulation, the real hardware will be assigned for executing the threads".

Dearth'242 states in Abstract, Lines 17-20 that all tests which are to **request reservations** (allocations) of **devices** (real hardware and not data) of the circuit simulation have requested from the hub such reservations (allocations) before any test proceeds.

Dearth et al. ('824) teaches at CL1, L39-42 a method and apparatus for arbitrating multiple, simultaneous requests for access to simulation **resource** (not data) which simultaneously prevents access collisions; at CL2, L46-48 that a protocol by which multiple simultaneous attempted interactions with a particular **component** (resource and not data) of the simulated circuit are arbitrated; at CL3, L8-11 that reservation of a device or component by a test refers to acquisition of access, which is exclusive with respect to other tests, to that device or component"; CL3, L57-60 that an efficient, repeatable arbitration mechanism for access to various components (not data) of a simulated circuit by multiple concurrently executing tests of the simulated circuit.

Levy et al. states at CL3, L2-5, "a method for assigning (allocating) registers (resource) for use by a multithreaded processor that is capable of executing instructions from a plurality of threads out-of-order"; at CL3, L11-13, "the renaming registers (resources) are dynamically allocated and assigned to a thread being processed by the multithreaded processor".

Conclusion

ACTION IS FINAL

22. Applicant's arguments with respect to claim rejections under 35 USC 103 (a) are not persuasive. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a).
Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

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A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

23. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dr. Kandasamy Thangavelu whose telephone number is 571-272-3717. The examiner can normally be reached on Monday through Friday from 8:00 AM to 5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Paul Rodriguez, can be reached on 571-272-3753. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to TC 2100 Group receptionist: 571-272-2100.

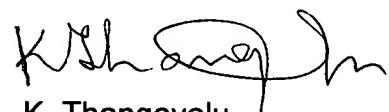
Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for

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published applications may be obtained from either Private PAIR or Public PAIR.

Status information for unpublished applications is available through Private PAIR only.

For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



K. Thangavelu
Art Unit 2123
June 29, 2006